

CLAIMS

What is claimed is:

- 1 1. An imaging error diffusion apparatus comprising:
2 a first thread having an error input and a pixel input and producing an error
3 output; and
4 at least one other thread each having a pixel input and an error input, the at least
5 one other thread producing an error output in response to the error output of the first
6 thread.

- 1 2. The apparatus as claimed in claim 1, wherein the at least one other thread is at
2 least two threads, where each of the other threads has an error input coupled to an
3 error output of another thread.

- 1 3. The apparatus as claimed in claim 1, wherein the first thread receives error data
2 of a previous row and pixel data of a current row and the at least one other thread
3 receives error data of the current row and pixel data of a subsequent row.

- 1 4. The apparatus as claimed in claim 1, wherein the apparatus is included within an
2 image signal processor.

- 1 5. The apparatus as claimed in claim 1, wherein the apparatus is included within a
2 digital media processor.

1 6. The apparatus as claimed in claim 1, wherein a total number of the first thread
2 and the at least one other threads is equal to or greater than a number of stages in an
3 error diffusion hardware pipeline.

1 7. The apparatus as claimed in claim 6, wherein the total number of the first thread
2 and the at least one other threads is equal to the number of stages in the error diffusion
3 hardware pipeline.

1 8. The apparatus as claimed in claim 7, wherein the total number of the threads and
2 the number of the stages is three.

1 9. The apparatus as claimed in claim 1, wherein each of the first thread and the at
2 least one other threads execute concurrently.

1 10. The apparatus as claimed in claim 1, wherein the first thread has a second error
2 input.

1 11. The apparatus as claimed in claim 10, wherein each of the at least one other
2 threads has a second error input.

1 12. The apparatus as claimed in claim 1, wherein each of the at least one other
2 threads has a second error input.

1 13. An imaging error diffusion method comprising:
2 receiving at a first thread an error input and a pixel input and producing an error
3 output; and
4 receiving at a second thread a pixel input and the error output of the first thread
5 and producing an error output in response to the error output of the first thread.

1 14. The method of claim 13, further comprising the first thread calculating an error
2 value for a current pixel based on the pixel input, the error input and at least one other
3 previously calculated error value within the first thread.

1 15. The method of claim 13, further comprising receiving at a third thread a pixel
2 input and the error output of the second thread and producing an error output in
3 response to the error output of the second thread.

1 16. The method of claim 13, wherein the first thread and the second thread execute
2 concurrently.

1 17. The method of claim 13, wherein the first thread receives a second error input.

1 18. The method of claim 17, wherein the second thread receives a second error
2 input.

1 19. The method of claim 13, wherein the second thread receives a second error
2 input.

1 20. A system comprising
2 a memory; and
3 a processor coupled to the memory; and
4 an imaging error diffusion apparatus comprising:
5 a first thread having an error input and a pixel input and producing an error
6 output; and
7 at least one other thread each having a pixel input and an error input, the
8 at least one other thread producing an error output in response to the error
9 output of the first thread.

1 21. The system as claimed in claim 20, wherein the error output of the first thread is
2 not stored in memory.

1 22. The system as claimed in claim 20, wherein the error output of the first thread is
2 not stored in any memory external to the threads.

1 23. The system as claimed in claim 20, wherein a total number of the first thread and
2 the at least one other threads is equal to or greater than a number of stages in an error
3 diffusion hardware pipeline included in the processor.

1 24. The system as claimed in claim 23, wherein the total number of the first thread
2 and the at least one other threads is equal to the number of stages in the error diffusion
3 hardware pipeline.

1 25. The apparatus as claimed in claim 24, wherein the total number of the threads
2 and the number of the stages is three.

1 26. The apparatus as claimed in claim 20, wherein each of the first thread and the at
2 least one other threads execute concurrently.

1 27. The system as claimed in claim 20, wherein the first thread has a second error
2 input.

1 28. The system as claimed in claim 27, wherein each of the at least one other
2 threads has a second error input.

1 29. The apparatus as claimed in claim 20, wherein each of the at least one
2 other threads has a second error input.